AND8174/D

NIS6111 Better ORing Diode Operation Notes

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APPLICATION NOTE

General Description

The NIS6111 is a simple and reliable device consisting of an integrated control IC with a low $R_{DS(on)}$ power MOSFET, using hybrid technology. It is designed to replace Schottky diodes in ORing applications to obtain higher system power efficiency. It can be connected to allow load sharing with automatic switchover of the load between two or more input power supplies. A single NIS6111 is able to run up to 20 A without any air flow. To meet high current requirement (i.e. 60 A), the NIS6111 is designed to drive more than four paralleled additional NTD110N02 MOSFETs. The unique package design of NIS6111 offers higher thermal efficiency to minimize cooling requirements.

This application note presents more details of the 30 A and 60 A demonstration boards. Both of them can be easily connected to power sources and loads for any test purpose.

Applications

Paralleled N + 1 Redundant Power Supplies
Telecommunications Power Systems
High−Reliability, Distributed Power Networks

NIS6111 Simplified Block Diagram

Reg_in (Pin 5): Input pin for internal voltage regulator.

Bias (Pin 2): Output of internal voltage regulator. It is 5.0 V under normal operating conditions. It provides power for internal components only. No external connections are necessary at this pin.

Gate (Pin 3): Gate driver output for internal and external N−Channel MOSFET. The gate turn on time is typically 22 nS.

Source (Pin 1): Power input, connected to the system power source output. This is the anode of the rectifier.

Drain (Pin 4): Power output, connected to the system load. This pin is the cathode of the rectifier and will be common to the cathodes of the other rectifiers, when used in a high side configuration.

UVLO Function: The UVLO is set for a trip point of 3.85 V rising and 3.65 V falling of the bias supply. Before the bias voltage reaches 3.85 V, UVLO is a logic “1”, which disables gate driver. The gate voltage remains at zero; as soon as the bias voltage reaches 3.85 V or more, the UVLO changes to logic “0”, and enables the gate driver. The gate voltage will then switch to 5.0 V if the device is forward biased (see Figure 2).

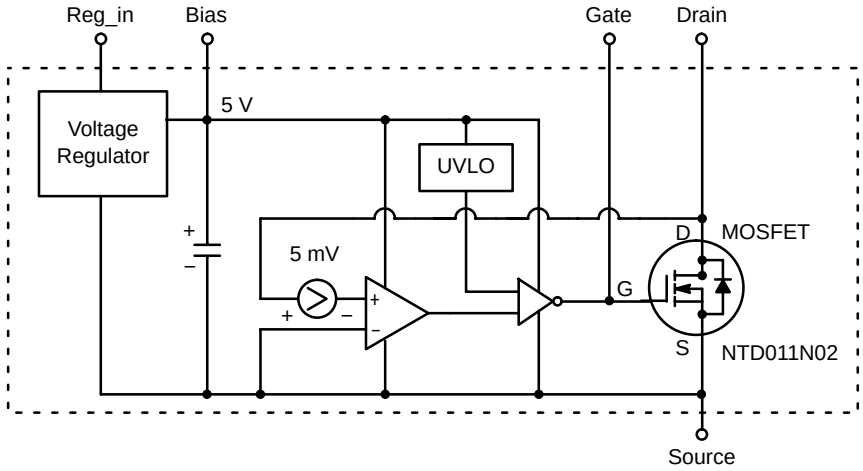

Figure 1.

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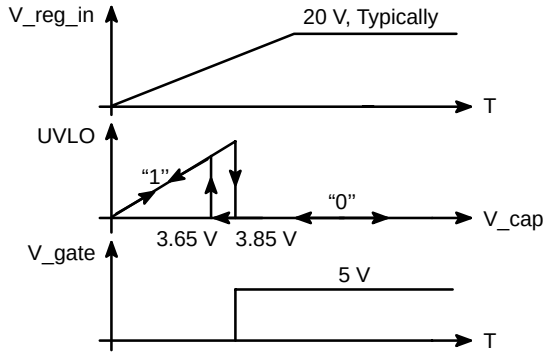


Figure 2.

NIS6111 Basic Operating Circuit and Sequence

To disable the UVLO circuit, V_reg_in has to be higher than the source pin by more than 6.0 V.

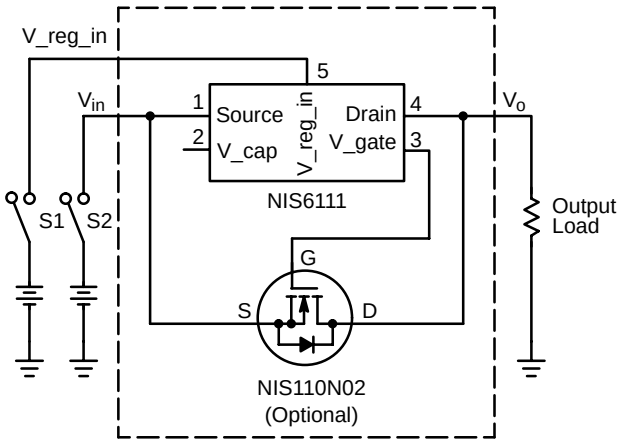


Figure 3. Basic Operation Circuit

Timing Sequence: It is recommended that V_reg_in be energized before the device is turned on, so that the control circuit can quickly respond to the correct polarity of the gate drive signal.

It is also possible to bring the V_reg_in pin and V_{in} up simultaneously. In this case the FET will be off until the UVLO reaches its threshold. Under this condition, the FET body diode will conduct as a normal rectifier would.

If the V_reg_in voltage comes up after the V_{in} supply, the FET body diode will conduct if it is forward biased. This will not damage the device as long as the power dissipation does not cause the maximum junction temperature for the NIS6111 to be exceeded.

Under no conditions should the V_reg_in pin go more negative than the source (anode) pin of this device. If that situation can occur, a signal diode should be connected in series with the V_reg_in pin.

In Table 1, the number of external MOSFETs is based on no air flow or heat sink. The test data is from the 60 A demonstration board. For system applications, the required number of external MOSFETs may be decreased due to the air flow in the system and external heat sink.

Table 1. Recommended Selection of External MOSFETs Based on Load Currents

Under No Air Flow and No Heat Sink Condition	
Recommended Selection	**Max Load Current Rating (A)**
Single NIS6111	20
NIS6111 and One NTD110N02	30
NIS6111 and Two NTD110N02	40
NIS6111 and Three NTD110N02	50
NIS6111 and Four NTD110N02	60

TEST CIRCUIT

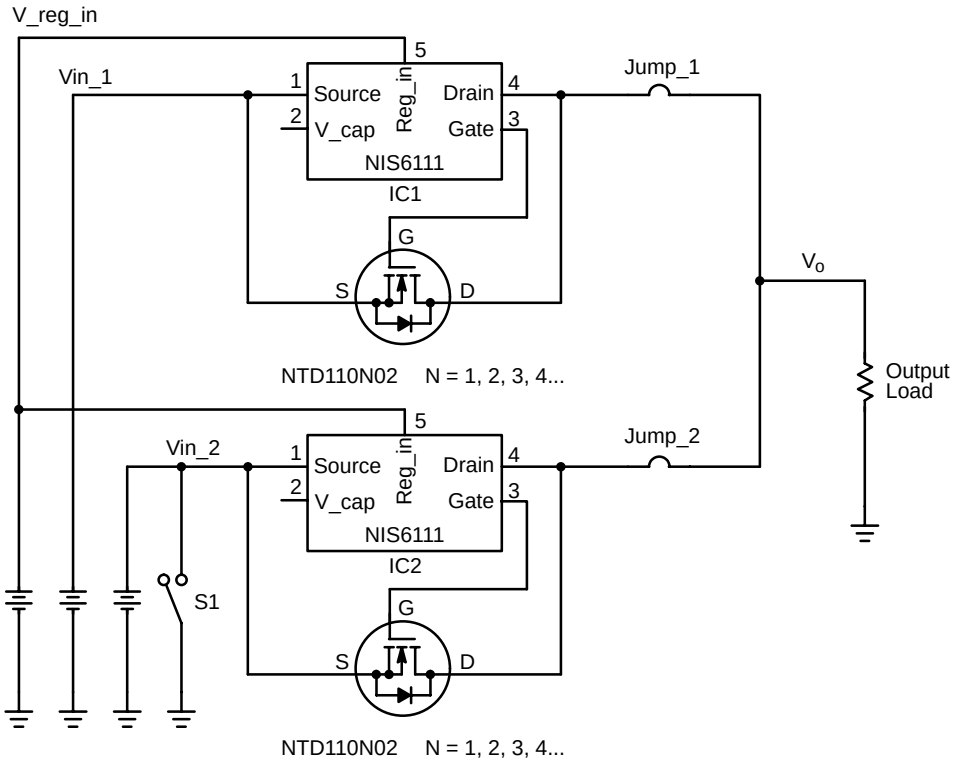


Figure 4. Test Circuit

Basic Test Circuit

The test circuit in Figure 4 is set to test peak reverse current and recovery time for multiple power source operation.

With Vin_2 > Vin_1, the load current will flow through IC2 and its paralleled MOSFETs. After switching on S1 (Shut Vin_2), IC1 and its paralleled MOSFETs will take over the power transfer path, and current will go through them instead of IC2 and its paralleled MOSFETs. Meanwhile, since V_o > Vin_2 (after shutting Vin_2) a small amount of reverse current will be forced to go through IC1 and its MOSFETs , which will terminate the conduction of this switch.

Since the NIS6111 does not have the reverse applied voltage protection (such as when Vin voltage is higher than Vreg_in's), it is needed to add a diode (e.g. 1N4148) in serial with Pin5 (Reg_in). Also, since the system has the noises, an RC snubber circuit between Pin1 (Source) and Pin4 (Drain) is strongly recommended, to avoid the gate signal ringing. The details can be seen in the schematics 30 A and 60 A demo boards as follows.

30 A DEMONSTRATION BOARD

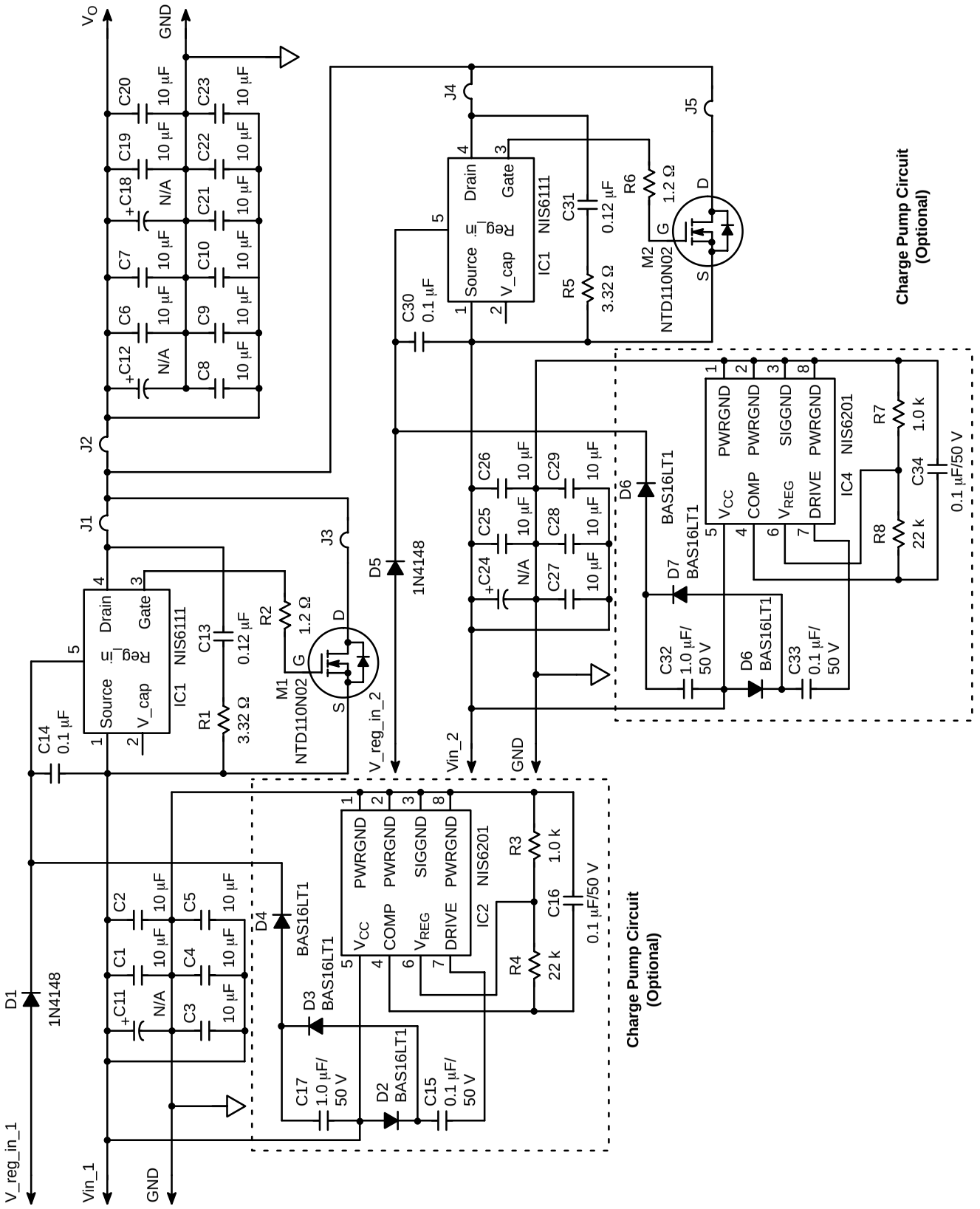
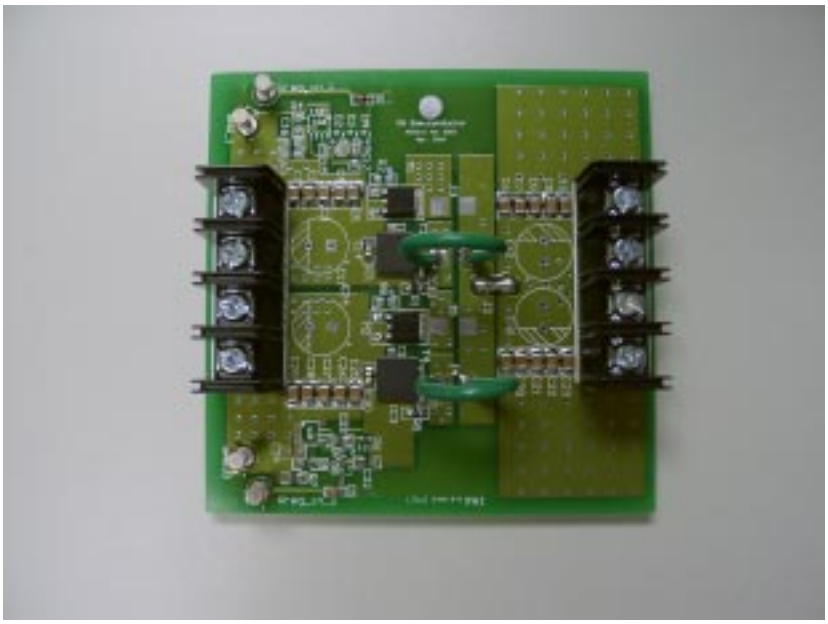


Figure 5. 30 A Demonstration Board Schematic

30 A DEMONSTRATION BOARD (continued)



NOTE: The selection of input and output capacitors vary, based on the PCB layout and the maximum load in the applications.

Figure 6.

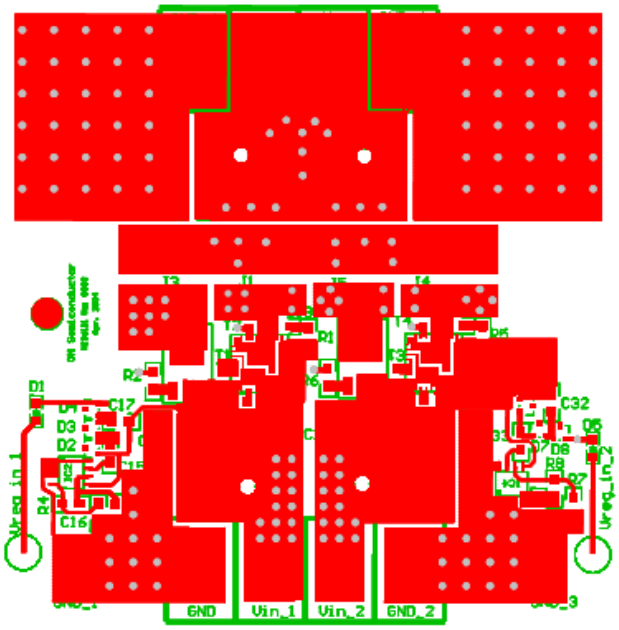


Figure 7. Top PCB Layout

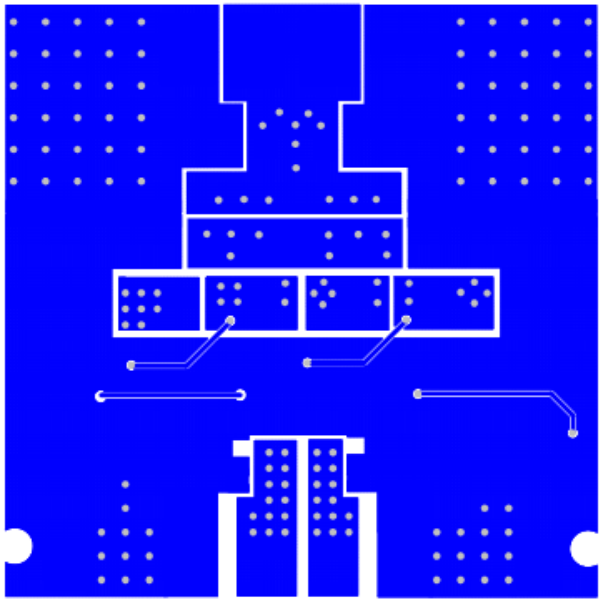


Figure 8. Bottom PCB Layout

30 A DEMONSTRATION BOARD (continued)

Table 2 and Figure 9 present the current sharing data at different load conditions.

Table 2. Current Sharing Test Results

Current Sharing Rating (A)		
Load Current	**NIS6111**	**NTD110N02**
2.0	1.1	0.9
5.0	2.7	2.3
10	5.4	4.6
15	8.0	7.0
20	10.5	9.5
25	13	12
30	16	14

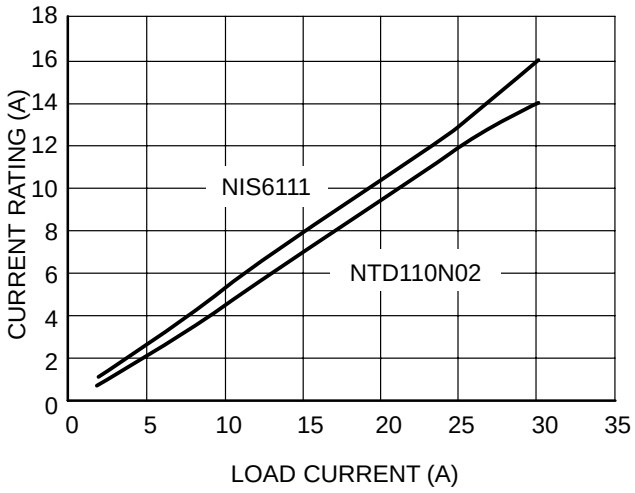


Figure 9. Current Sharing vs. Load Current

Table 3. Thermal Test Results

Under No Air Flow and No Heat Sink Condition		
Thermal Data		
Load Current (A)	**NIS6111 Max Temp (°C)**	**NTD112N02 Max Temp (°C)**
30	83	78

Reverse Current and Recovery Time Test Results

Figure 10 shows the waveforms at a typical load condition (10 A). The reverse current is 1.5 A, the recovery time is 140 nS.

In Figure 10, the slope (di/dt) of the waveform (Ch3) is a function of the parasitic inductance and capacitance of the system. With increasing the current path length and the component spaces on the PCB, decreasing the slope (di/dt).

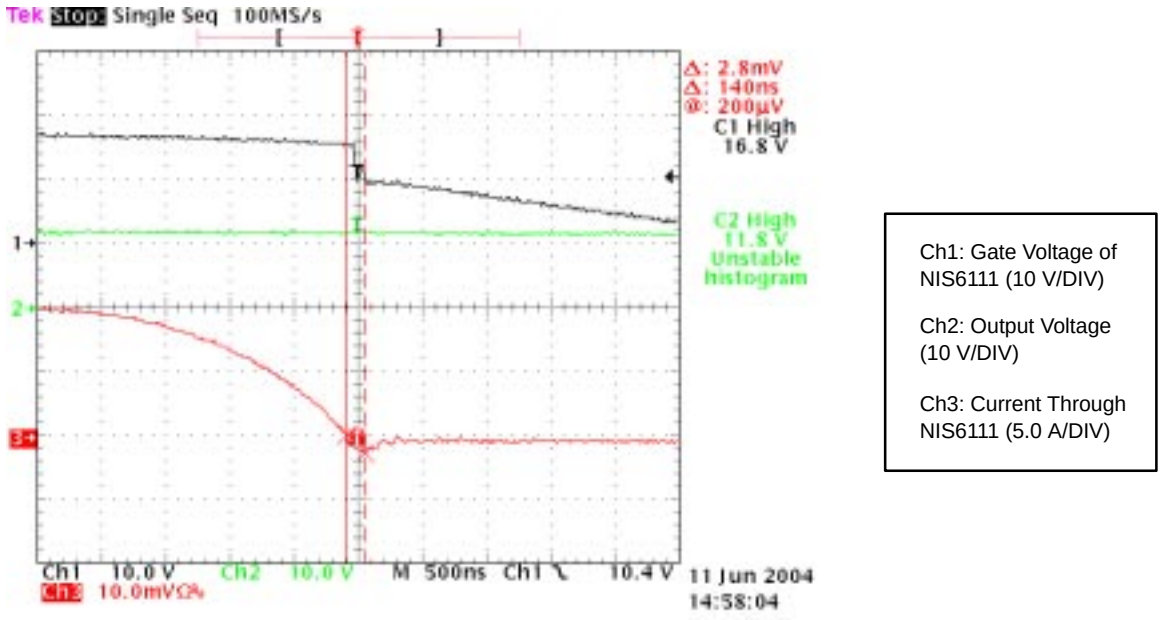


Figure 10.

60 A DEMONSTRATION BOARD

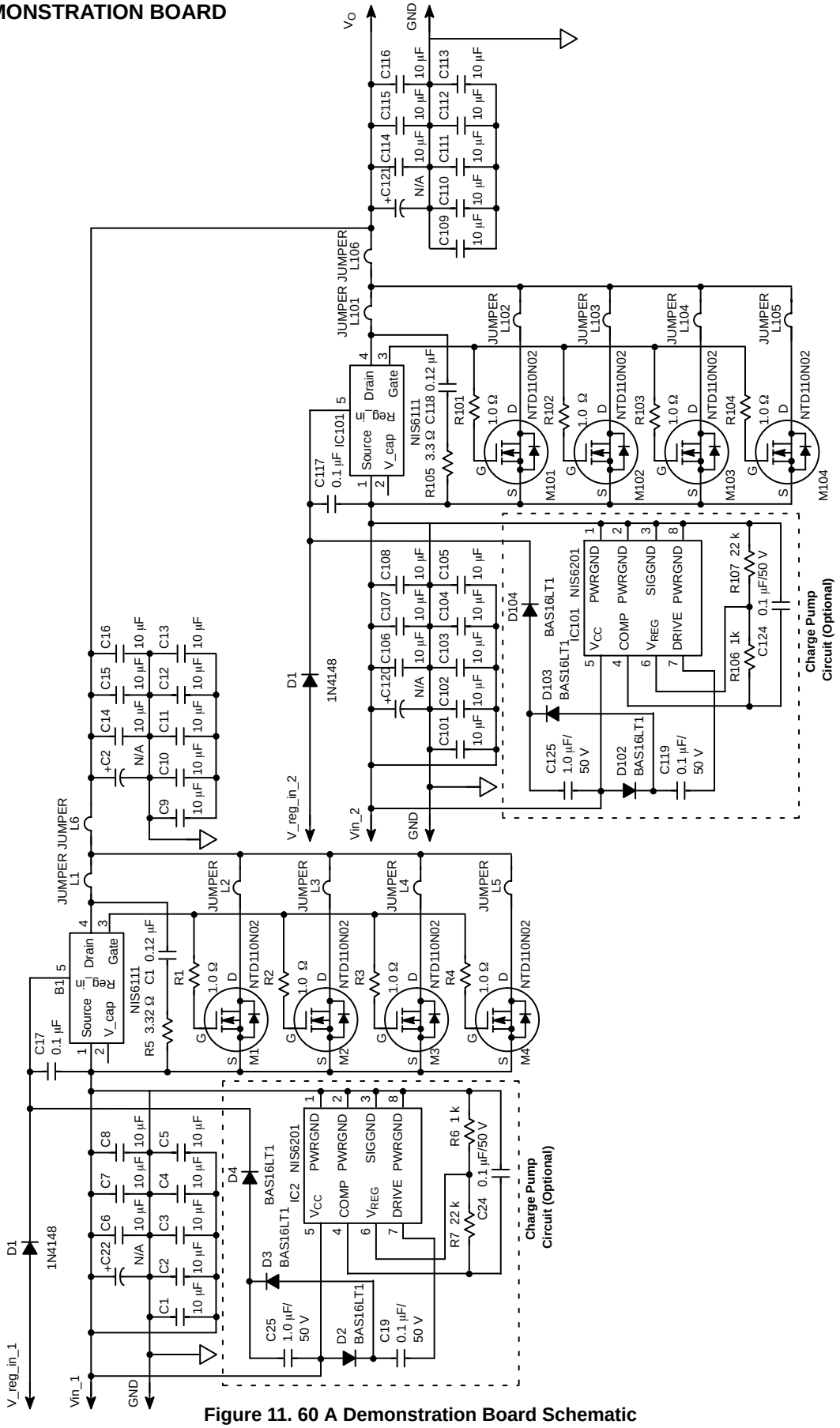


Figure 11. 60 A Demonstration Board Schematic

60 A DEMONSTRATION BOARD (continued)

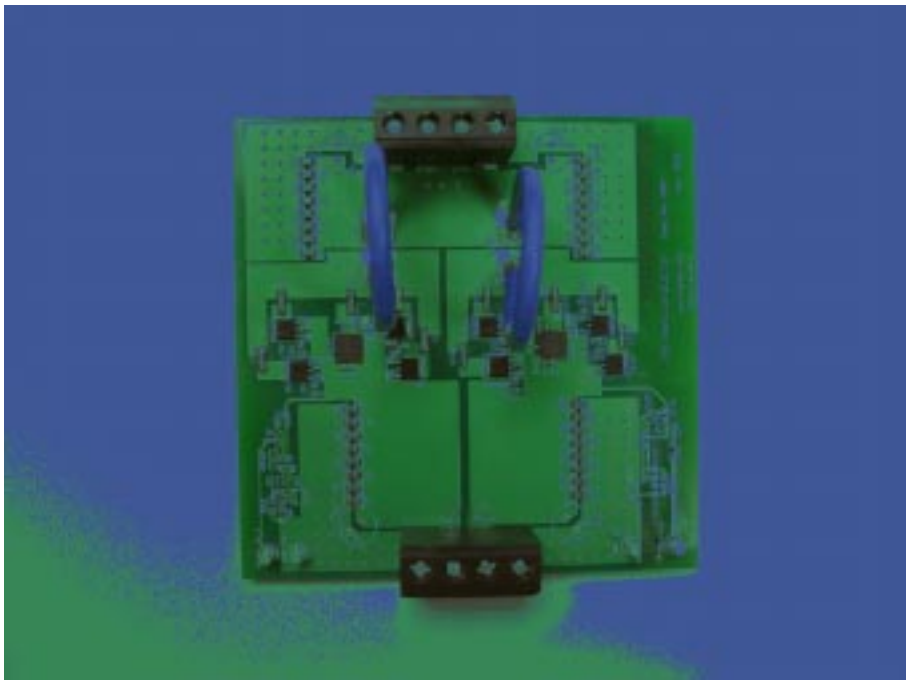


Figure 12.

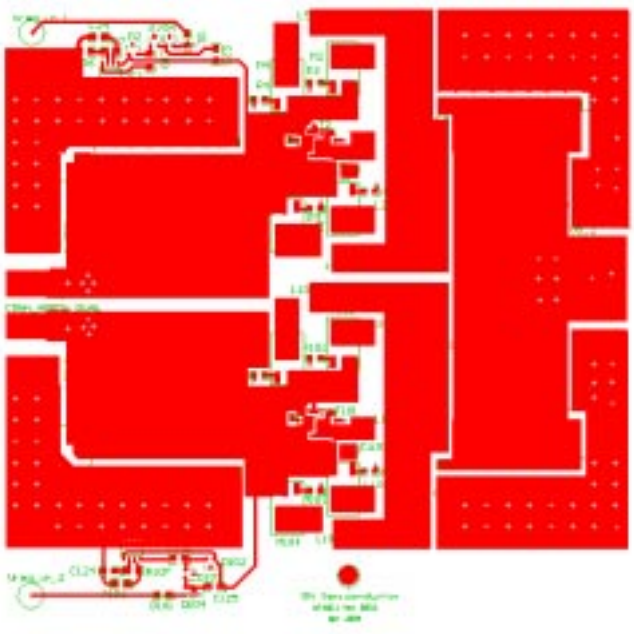


Figure 13. Top PCB Layout

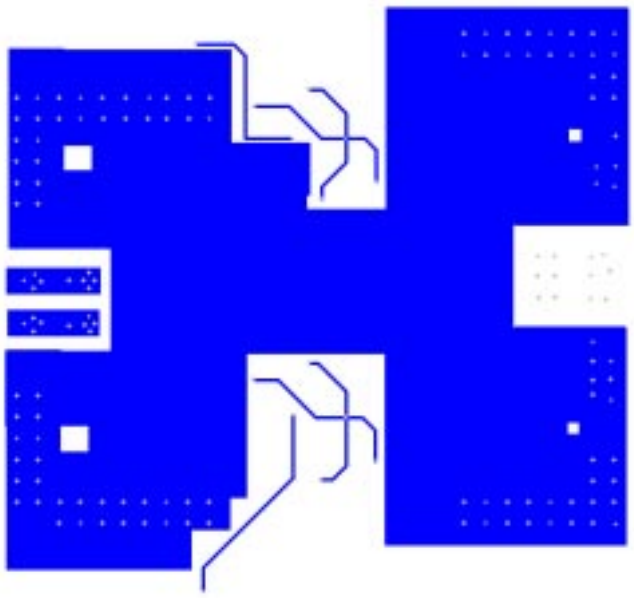


Figure 14. Bottom PCB Layout

60 A DEMONSTRATION BOARD (continued)

Table 4 and Figure 15 present the current sharing data at different load conditions.

Table 4. Current Sharing Test Results

Current Sharing Ratings (A)				
Io (A)	**NIS6111**	**M101**	**M102**	**M103**
5.0	1.3	1.1	1.1	1.2
10	2.6	2.4	2.2	2.4
15	4.0	3.6	3.4	3.6
20	5.4	4.8	4.8	5.0
25	6.8	5.8	6.0	6.0
30	8.4	7.4	7.0	7.4
35	9.6	8.4	8.2	8.6
40	11	9.7	9.5	9.8
45	12.4	10.8	10.6	11
50	13.5	12	11.5	12
55	15	13	12.5	13

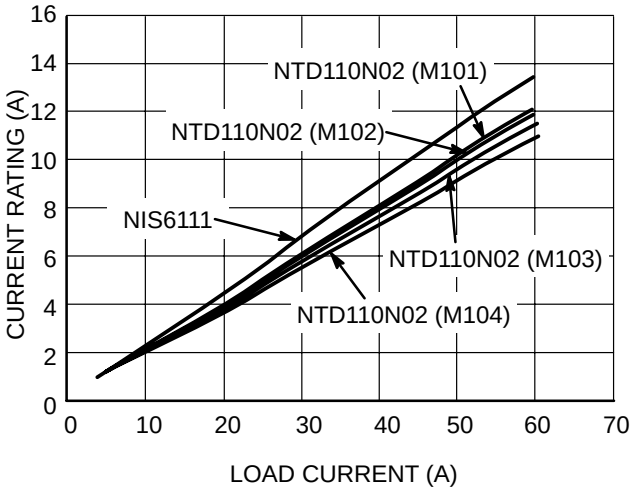


Figure 15. Current Sharing vs. Load Currents

Table 5. Thermal Test Results

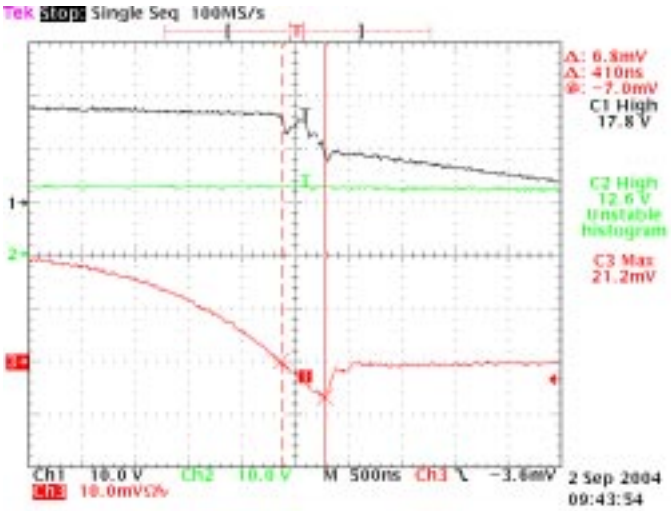
Under No Air Flow and No Heat Sink Condition		
Devices	**Max Load Current Rating (A)**	**Max Thermal Rating Typical**
Single NIS6111	20	65
NIS6111 and One NTD110N02	30	78
NIS6111 and Two NTD110N02	40	81
NIS6111 and Three NTD110N02	50	82
NIS6111 and Four NTD110N02	60	86

Reverse Current and Recovery Time Test Results

Figure 16 presents the waveforms at a typical load condition (10 A). The reverse current is 3.4 A, the recovery time is 440 nS.

Conclusion

The application note describes the NIS6111 device operation and the details of 30 A and 60 A demonstration boards.



Ch1: Gate Voltage of NIS6111 (10 V/DIV)

Ch2: Output Voltage (10 V/DIV)

Ch3: Output Current (5.0 A/DIV)

Figure 16.

PUBLICATION ORDERING INFORMATION

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