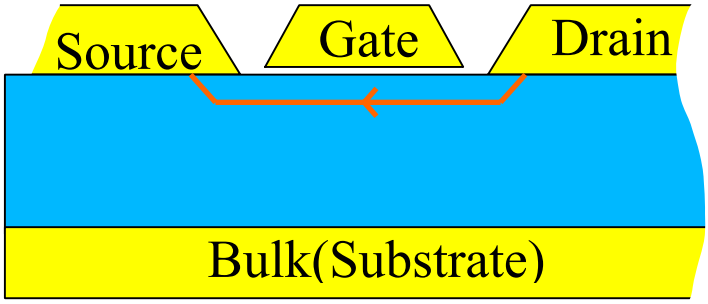
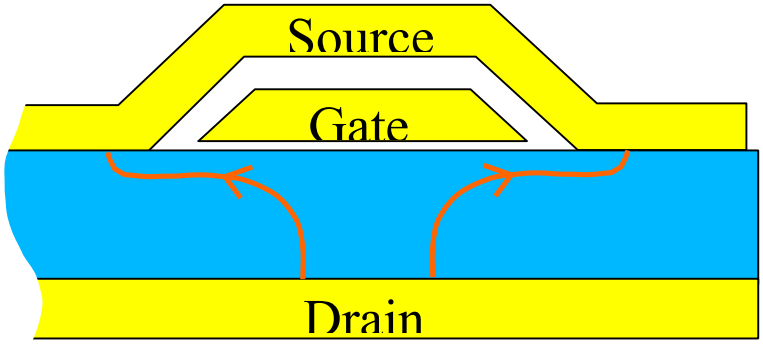
# LTspice build in VDmos model.

## *Introduction (from the help file)*

The discrete vertical double diffused MOSFET transistor (VDMOS) popularly used in board level switch mode power supplies has behavior that is qualitatively different than the monolithic MOSFET models. In particular, (i) the body diode of a VDMOS transistor is connected differently to the external terminals than the substrate diode of a monolithic MOSFET and (ii) the gate-drain capacitance (Cgd) non-linearity cannot be modeled with the simple graded capacitances of monolithic MOSFET models. In a VDMOS transistor, Cgd abruptly changes about zero gate-drain voltage (Vgd). When Vgd is negative, Cgd is physically based a capacitor with the gate as one electrode and the drain on the back of the die as the other electrode. This capacitance is fairly low due to the thickness of the non-conducting die. But when Vgd is positive, the die is conducting and Cgd is physically based on a capacitor with the thickness of the gate oxide.

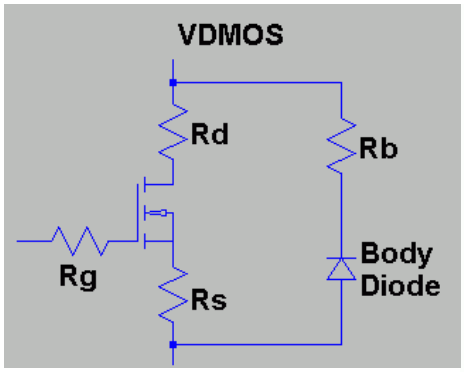


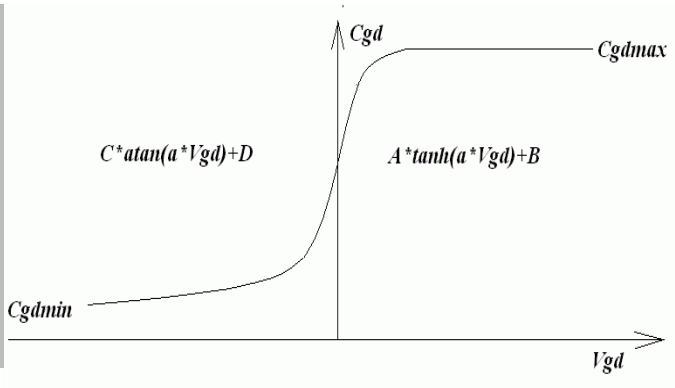

Normal Monolithic MOSFET
(Used in IC's)




VDMOS
(Discrete Power MOSFET)

Traditionally, elaborate subcircuits have been used to duplicate the behavior of a power MOSFET. A new intrinsic spice device was written that encapsulates this behavior in the interest of compute speed, reliability of convergence, and simplicity of writing models. The DC model is the same as a level 1 monolithic MOSFET except that the length and width default to one so that transconductance can be directly specified without scaling. The AC model is as follows. The gate-source capacitance is taken as constant. This was empirically found to be a good approximation for power MOSFETS if the gate-source voltage is not driven negative. The gate-drain capacitance follows the following empirically found form:



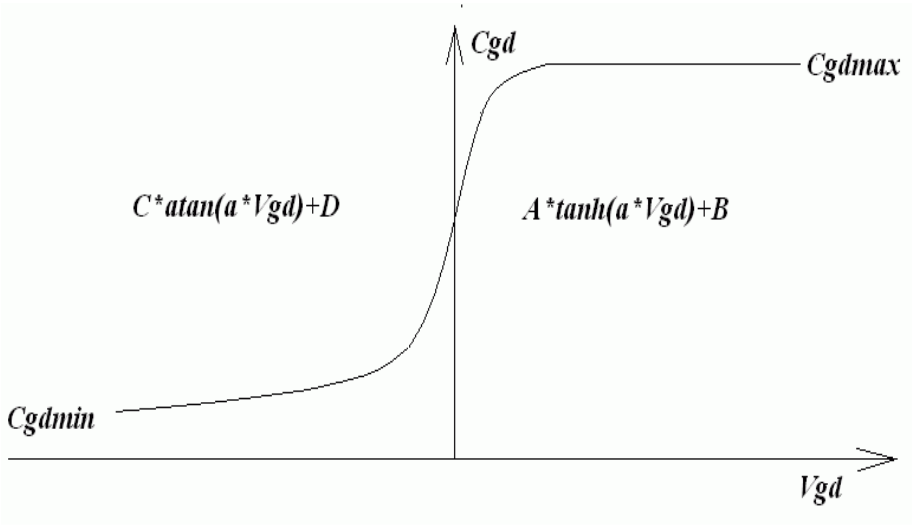




For positive Vgd, Cgd varies as the hyperbolic tangent of Vgd. For negative Vdg, Cgd varies as the arc tangent of Vgd. The model parameters a, Cgdmax, and Cgdmax parameterize the gate drain capacitance. The source-drain capacitance is supplied by the graded capacitance of a body diode connected across the source drain electrodes, outside of the source and drain resistances.

Parameters used in VDmos model to describe the AC behavior are:

| | |
|---|---|
| Cgs | Gate-source overlap capacitance |
| Cgdmin | Minimum non-linear G-D capacitance |
| Cgdmax | Maximum non-linear G-D capacitance |
| a | non-linear Cgd |
| Cjo | Body diode junction capacitance |

## *Detailed description of the VDmos nonlinear capacitor Cgd. (datasheet Crss value)*




The variables A, B, C and D are internally calculated depending on Cgdmin and Cgdmax parameter values. The parameter A and C are the slope of the atan and tanh curves @ Vgd = 0. The variables D and B determine the crossover value @ Vgd = 0.

If you carefully at the graph you can easily say that:

Parameter D must be the same as B because with Vgd = 0 the transition from the left to the right part of the graph must match. The value here is unknown at this point and therefore a new variable is introduced: Crossover . See this as a gain. The data sheet Crssmax value is also measured at this point.

$$Crss\max = D = B = Crossover * Cgd\max$$

Now for parameter A. We know that tanh(oo) is 1 and A must be a function of Crossover and Cgdmax.

With Vgd is infinite:

$$Cgd\max = A + Crossover * Cgd\max$$
$$A = -Crossover * Cgd\max + Cgd\max$$
$$A = (1 - Crossover) * Cgd\max$$

The variable C controls the Cgdmin value. The C*atan(-oo)+D must reach to Cgdmin.

$$Cgd\min = C * a\tan(-oo) + Crossover * Cgd\max$$
$$C * a\tan(oo) = Crossover * Cgd\max - Cgd\min$$
$$C = \frac{Crossover * Cgd\max - Cgd\min}{a\tan(oo)}$$

The variable Crossover can be found by matching the slope of the left and right part of the graph at Vgd = 0. The slope is C and A.

$$A = C$$

$$(1 - Crossover) * Cgd\max = \frac{(Crossover * Cgd\max - Cgd\min)}{a\tan(oo)}$$

$$Crossover = \frac{Cgd\min \Big/ a\tan(oo) + Cgd\max}{Cgd\max \Big/ a\tan(oo) + Cgd\max}$$

$$Crossover = \frac{Cgd\min + a\tan(oo) * Cgd\max}{Cgd\max * (1 + a\tan(oo))}$$

$$Crossover = \frac{\frac{Cgd\min}{Cgd\max} + a\tan(oo)}{1 + a\tan(oo)}$$

The term Crossover * Cgdmax is used in A, B, C and D

$$Crossover * Cgd\max = \frac{Cgd\min + a\tan(oo) * Cgd\max}{1 + a\tan(oo)}$$

For A:

$$A = Cgd\max - \frac{Cdg\min + a\tan(oo) * Cgd\max}{1 + a\tan(oo)}$$

For C:

$$C = \frac{\frac{Cgd\min + a\tan(oo) * Cgd\max}{1 + a\tan(oo)} - Cgd\min}{a\tan(oo)}$$

$$C = \frac{\frac{Cgd\min}{a\tan(oo)} + Cgd\max}{1 + a\tan(oo)} - \frac{Cgd\min}{a\tan(oo)}$$

Put everything together to complete the left and right functions of the Cgd graph.

For Vgd<0:

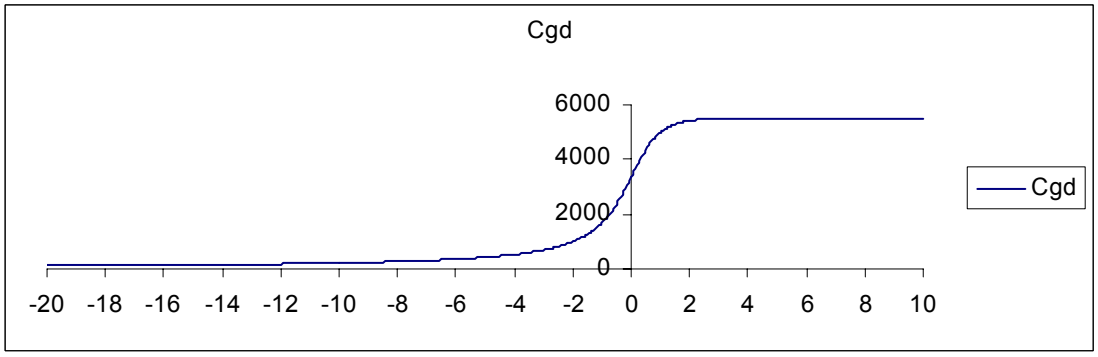
$$Cgd = \left( \frac{\frac{Cgd\ \min}{a\tan(oo)} + Cgd\ \max}{1 + a\tan(oo)} - \frac{Cgd\ \min}{a\tan(oo)} \right) * a\tan(a * Vgd) + \frac{Cgd\ \min + a\tan(oo) * Cgd\ \max}{1 + a\tan(oo)}$$

For Vgd>0

$$Cgd = \left( Cgd\ \max - \frac{Cdg\ \min + a\tan(oo) * Cgd\ \max}{1 + a\tan(oo)} \right) * \tanh(a * Vgd) + \frac{Cgd\ \min + a\tan(oo) * Cgd\ \max}{1 + a\tan(oo)}$$

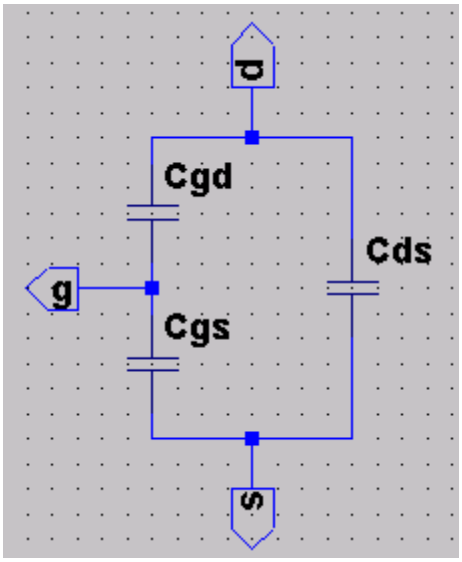
Example using the formulas above in excel:

Cgdmin=7 Cgdmax=5500




The parameter Cgdmax for the nonlinear gate drain cap is not the datasheet Crssmax value but a factor higher. The datasheet Crssmax value is read from the typical capacitance graph at Vgs = 0 and Vds = 0.

## *The datasheet Crss, Ciss and Coss parameters for the VDmos device.*




The datasheet supplies information for the charge model above in the form of Crss, Ciss and Coss. The values in the datasheet are measured with a gate source voltage of 0V and drain source voltage of 25V.
The definition of Crss, Ciss and Coss are as follows:

$$Crss = Cgd$$

$$Coss = Cds + \frac{Cgd * Cgs}{Cgd + Cgs}$$

$$Ciss = Cgs + Cgd$$

Rewrite the above equations and find the Cgd, Cgs and Cds.

$$Cgd = Crss$$

$$Cds = Coss - \frac{Crss * (Ciss - Crss)}{Crss + Ciss - Crss}$$

$$Cgs = Ciss - Crss$$

Later we see that the Cds formula is not correct because of the nonlinearity of it. The formula is only correct at Vds is 25V and it will be used to calculate the nonlinearity parameter m of the body diode.
Fortunately, the gate drain cap is the datasheet Crss value and there is a graph in the datasheet that shows this capacitance value as a function of the drain source voltage.

Now most of the VDmos parameters are available. The Cjo parameter is Cds. Most of the cases the datasheet Crss is the VDmos parameter Cgdmin but be careful. It's better to check that Crss in the graph at Vds=25V is the same as at Vds max. With the coolmos 20n60c3 from infinion it is not the case.

Example Coolmos 20n60C3:

Crss=50p Ciss=2400p Coss=780p
Read from the graph:
Crssmin=7p Crssmax=2000p

To supply the VDmos model with the desired Cgdmax value some calculation has to be done because the Crssmax value in the graph is **not** Cgdmax of the VDmos parameter.
The datasheet does not supply information about the parameter Cgdmax, but a difficult to read Crss value in the capacitance graph at Vds and Vgs is 0. The Crssmax value in the datasheet graph is D=B=Crossover*Cgdmax for the VDmos model.

If we take the formulas for A and C and fill in for Crossover*Cgdmax=Crssmax and we know that A=C we can find a function to calculate Cgdmax:

$$A = (1 - Crossover) * Cgd\max = Cgd\max - Crss\max$$
$$C = (Crossover * Cgd\max - Cgd\min) / a\tan(oo) = (Crss\max - Cgd\min) / a\tan(oo)$$
$$A = C$$
$$Cgd\max - Crss\max = (Crss\max - Cgd\min) / a\tan(oo)$$

$$Cgd\max = Crss\max + (Crss\max - Cgd\min) / a\tan(oo)$$

Note that Cgdmin is the same as Crssmin, preferably the graph value at Vds is very high.

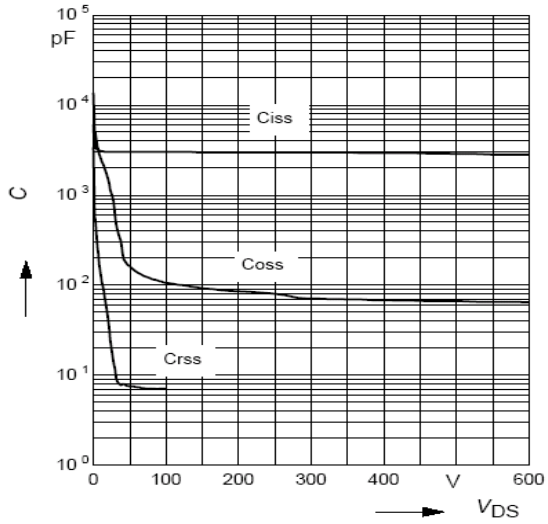
Now all the AC parameters for the VDmos can be calculated by means of datasheet values except for the “a” parameter that has to be fine-tuned. Most of the time the default value of 1 will do.

Here a summary of the VDmos AC parameters:

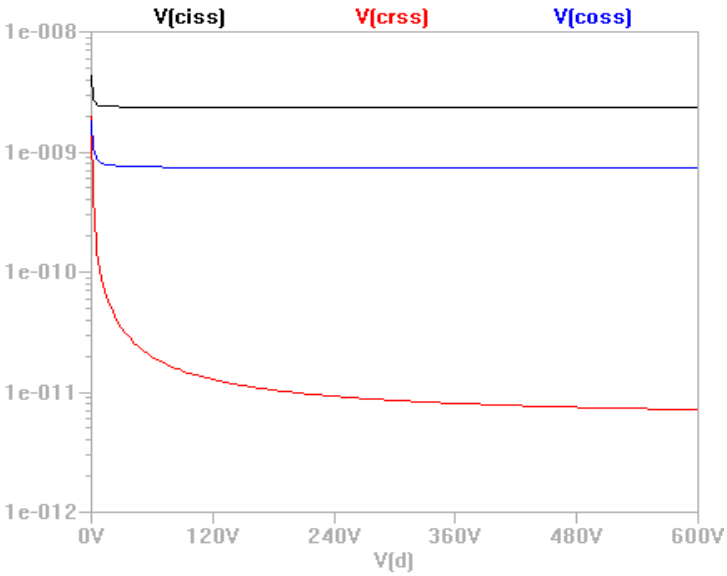
$$Cds_{25V} = Coss - \frac{Crss * (Ciss - Crss)}{Ciss}$$
$$Cgs = Ciss - Crss$$
$$Cgd\min = Crss\min$$
$$Cgd\max = Crss\max + (Crss\max - Cgd\min) / a\tan(oo)$$

## *Simulation results with the coolmos 20N60C3 as an example.*

For this device the following datasheet values has been found:
Crss=50p Ciss=2400p Coss=780p @ Vds=25V
from the graph:
Crssmin=7p Crssmax=2000p




The Vdmos parameters used are:
Cgdmin=7p
Cgdmax= 3270p
Cjo=731p
Cgs=2350p
a=1.5 (is tuned to fit the slope of the crss with the datasheet graph)



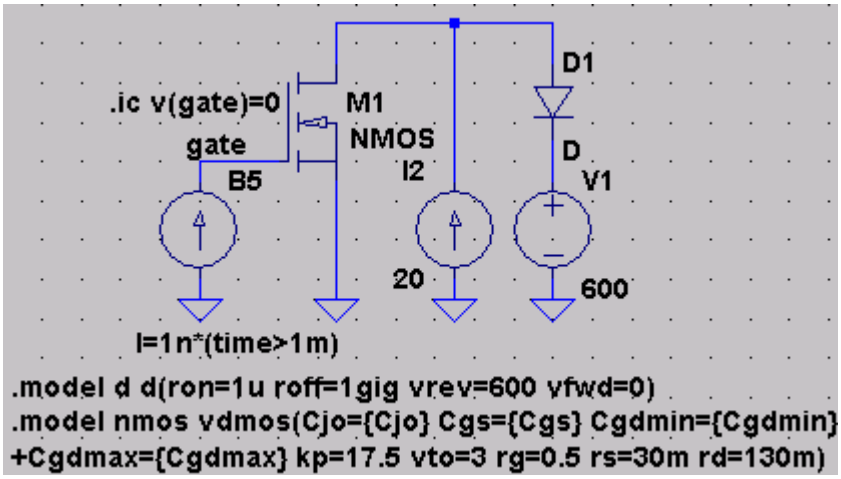

The Coss is way off. The nonlinearity of this cap is modulated in LTspice but not shown here because it is not taken into consideration with this simulation. The nonlinear Cds is described in the body diode section.

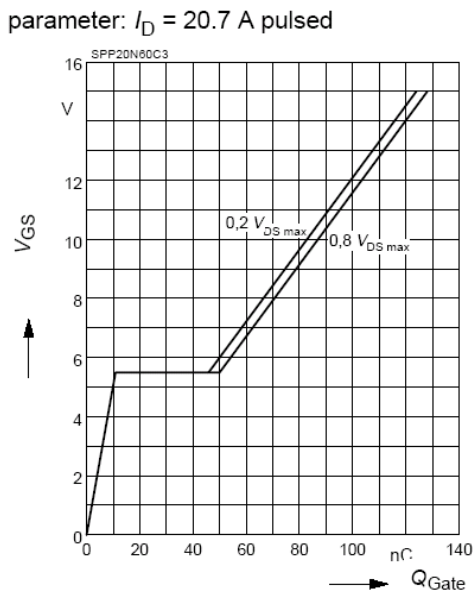
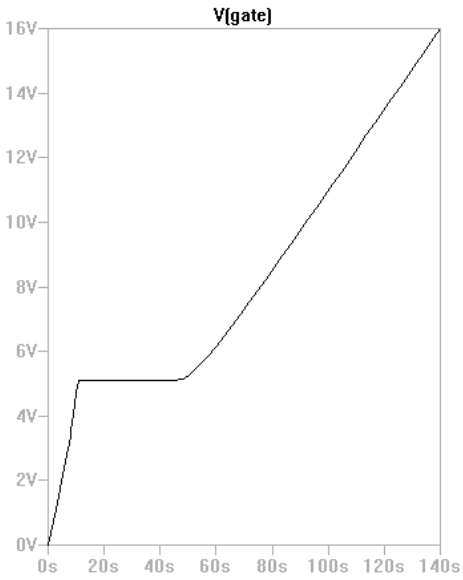
## *Workbench measurement results for the 20N60C3:*

It is too difficult to read the Crssmax value from the datasheet graph so I measured it using a simple cap meter.
Measured gate drain cap with gate shorted to source: 14nF
Actual Cgd=Cmeas-Cds= 14nF - ? = ?
The Cds is highly nonlinear and cannot be determent so shorted gate source measurements give no good Cgd value.
Measured gate drain cap with drain shorted to source: 6nF
Actual Cgd=Cmeas-Cgs= 6.3nF- 2.35nF = 3.65nF

So the Crssmax @ Vds=Vgs=0 is about 3.6nF

Test circuit to plot the Qgstotal:




| Datasheet plot of the Qgs | Simulated plot of the Qgs |
|---|---|
|  |  |



The right graph show time on the Y axis this is the same as Q in nC because the current source charging the gate is 1nA. (Q=i*t)

## *DC characteristics of the VDmos*

In order to make a model from datasheet we have to know the how Ltspice handles the dc parameters. The help file reveres to the level 1 model parameters.

The LEVEL 1 MOSFET model should be used when accuracy is less important than simulation turn-around time. For digital switching circuits, especially when only a "qualitative" simulation of timing and function is needed, LEVEL 1 run-time can be about half that of a simulation using the LEVEL 2 model. The agreement in timing is approximately 10%. The LEVEL 1 model, however, results in severe inaccuracies in DC transfer functions.

LEVEL 1 Model Equations

Cuttoff region: Vgs<Vth
Id=0
Linear Region: Vds<Vgs-Vth
Id=KP* W/L * (1+LAMBDA*Vds)*(Vgs-Vth-Vds/2)*Vds
Saturation Region: Vds>Vgs-Vth
Id=KP/2 * W/L * (1+LAMBDA*Vds)*(Vgs-Vth)^2

The saturation region is useless because for a switch you will not operate the device in this region. Then I played around with the formula for the linear region and could not get an Rdson fit. Make it fit with Rs and Rd (high KP value). Now Rs also determents the transfer characteristics and this makes everything a lot easier. If you take a look at the models shipped with LTspice, you see they also uses a high KP value and looks like the fets are matched with the Rs and Rd.

With this in mind I dropped a few things out of the formula that has little effect. W/L is useless because the default is ok and this makes it 1
LAMBDA is for the sat region and is not interesting, so can be zero. The Vgs/2 part is compared to (Vgs – Vto) has no meaning full contribution.
What's left is:

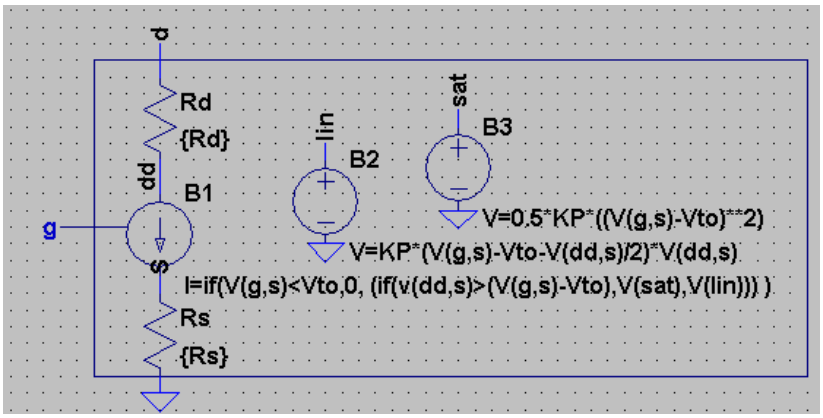
For the linear region:

Id=KP(Vgs-Vto)Vds

For the saturation region:

Id=0.5*KP * (Vgs-Vto)^2

The model of the level one mosfet is tested in Ltspice using this circuit:




The behaviour source looks at the 'internal' drain and source connections. The formulas must be extended with Rs and Rd.

Saturation region:

Id = 0.5*KP(Vg-Id*Rs-Vto)^2

Linear region:

Id=KP(Vg-Id*Rs-Vto)*(Vd-Id*(Rd+Rs)

The datasheet transfer characteristics graph is measured with the device in saturation region. We can use the formula for saturation region to calculate Rs:

Rs=(Vg-sqrt(2*Id/KP)-Vto)/Id

So with values from the transfer graph I have Vgsmax=7.5V with Idmax=70A.
Rs=(Vgsmax-sqrt(2*Idmax/Gfs)-Vth)/Idmax

Now for Rd. This can be calculated using Rs and Rdson. Rdson is shown in the output characteristics graph in the linear region so we use the formula for the linear region.

Rdson matching in linear region:
Id=KP(Vgs-Vto-Vds/2)*Vds

With Vd=1. Id=1/Rdson.
Id=KP(Vg-Id*Rs-Vto)*(Vd-Id*(Rd+Rs)

Rd=Rdson - 1/(KP*(Vg-Rs/Rdson-Vto)) - Rs
Rdson = Rs+1/KP(Vg- Rs/Rdson -Vto)+Rd

With Vg =10V and Vto=Vth: and KP=Gfs
Rd=Rdson-Rs-1/Gfs(10- Rs/Rdson -Vth)

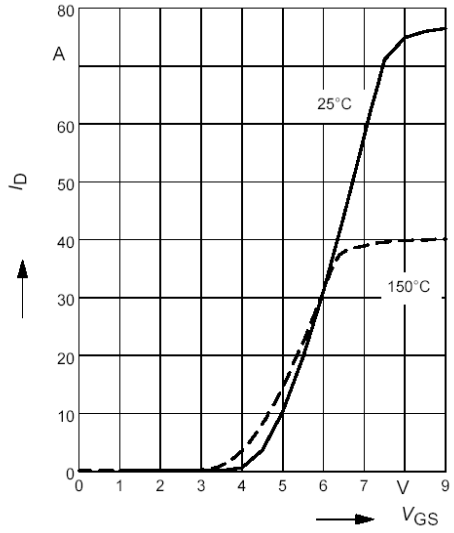
## *Simulation results DC characteristics.*

To verify the dc characteristics, simulations have done with the newly extracted parameters from data sheet.
The following parameters were used:

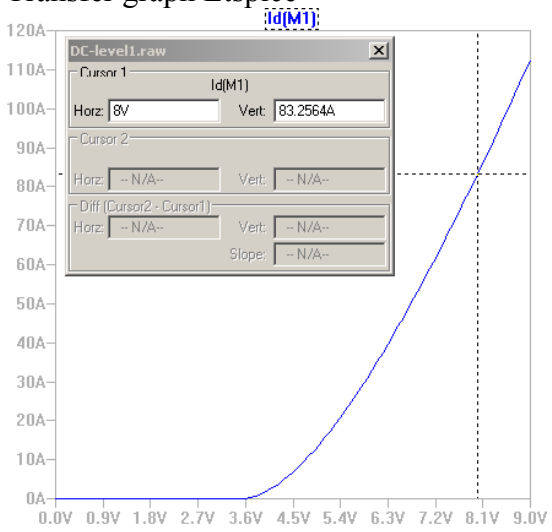
The datasheet trans-conductance Gfs=17.5
KP=17.5
Gate source threshold voltage Vth=3.5
Vto=3.5

Rdson = 0.16 and from the transfer graph Idmax=70A with Vgsmax=7.5V
Rs=(Vgsmax-sqrt(2*Idmax/Gfs)-Vth)/Idmax =0.017
Rd= Rdson-Rs-1/Gfs(10- Rs/Rdson -Vth)=0.134

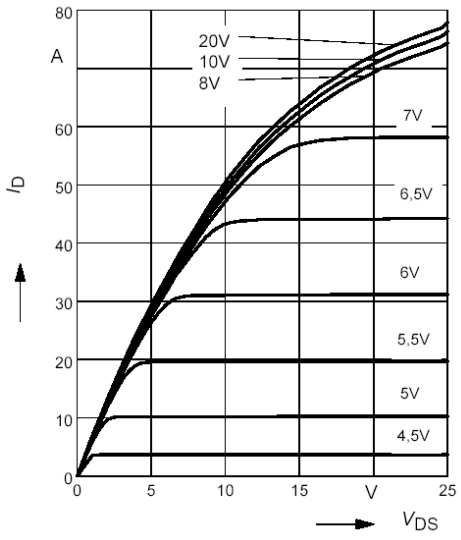
Transfer graph datasheet



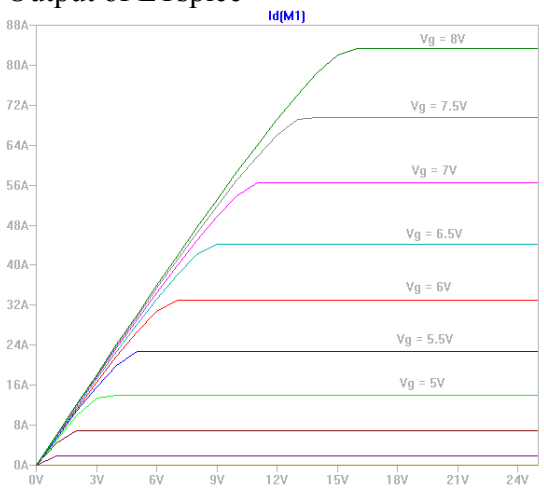

Transfer graph Ltspice




Output graph datasheet




Output of LTspice



The generated spice model matches the output characteristics and the transfer characteristics very well except for drain currents higher then 80A. But this is not a problem due to the fact it the device is specified for 20A max.

## *Body diode DC characteristics*

Generally, the diode dc characteristic is described using the following function.

$$Vd = Id * Rb + \frac{nkT}{q} \ln\left(\frac{Id}{Is} + 1\right)$$

Rb can now easily be calculated if we know the forward voltage and current.

$$\frac{Vd}{Id} = Rb + \frac{nkT}{Id * q} \ln\left(\frac{Id}{Is} + 1\right)$$

$$Rb = \frac{Vd}{Id} - \frac{nkT}{Id * q} \ln\left(\frac{Id}{Is} + 1\right)$$

Now the datasheet provides some information we can use to put in the formula but the exact behavior of the body diode forward voltage, as function of the forward current is probably not correct. This is not a problem because in normal use of the Vdmos, the body diode is mainly a freewheel diode for a zero voltage switching converter. A workable approach is in this case good enough.

The datasheet gives the parameter Is in the form of “zero gate voltage drain current” at the maximum drain source voltage and is called Idss. The value varies from several nA to a few uA.

Is=Idss

The Id here in the formula is the datasheet “inverse diode continues forward current” and is called Is.

Id=Is

With the continues forward current comes a voltage drop and is the datasheet “inverse diode forward voltage” and is called Vsd.

Vd=Vsd

## *Body diode AC characteristics*

For the nonlinear capacitor, the Cgd is a function of Cjo and Vds.

$$Cds = Cjo * \left(1 + \frac{Vds}{Vj}\right)^{-m}$$

We know the Cds when Vds is 25V. If the Cds is known for Vds is 0V than a better curve fit with the datasheet Coss can be made because the parameter m can be calculated.

For Vds is 0 the Cds=Cjo.

For Vds is 25V.

$$\frac{Cds_{25V}}{Cjo} = \left(1 + \frac{25}{Vj}\right)^{-m}$$

$$\log\left(\frac{Cds_{25V}}{Cjo}\right) = -m * \log\left(1 + \frac{25}{Vj}\right)$$

$$m = \frac{-\log\left(\frac{Cds_{25V}}{Cjo}\right)}{\log\left(1 + \frac{25}{Vj}\right)}$$

The parameter m can be calculated to match the nonlinear Cds better with the datasheet. The parameter Vj is default 0.75. Cjo is the maximum Cds at Vds=0.
To calculate the Cjo from Coss and Crss values we need to know these values were Vds is zero. Cgs must also be known. This has been calculated before using Cgs=Ciss-Crss datasheet table values (measured @ Vds=25V)

So Cjo is than

$$Cjo = Coss\max - \frac{Crss\max * Cgs}{Crss\max + Cgs}$$

Now for the nonlinear part of the Cds we must know the parameter m to fit the simulation with the datasheet Coss at Vds is 25V.

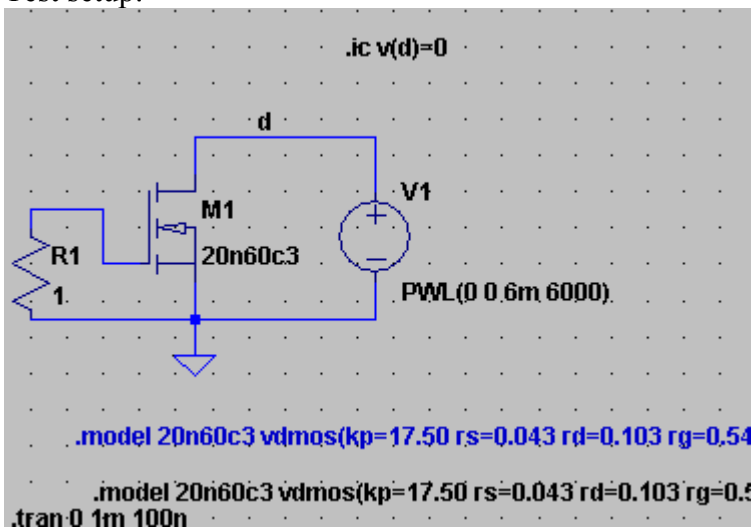
$$m = \frac{-\log\left(\frac{Cds_{25V}}{Cjo}\right)}{1.5357}$$

With Cds at 25V

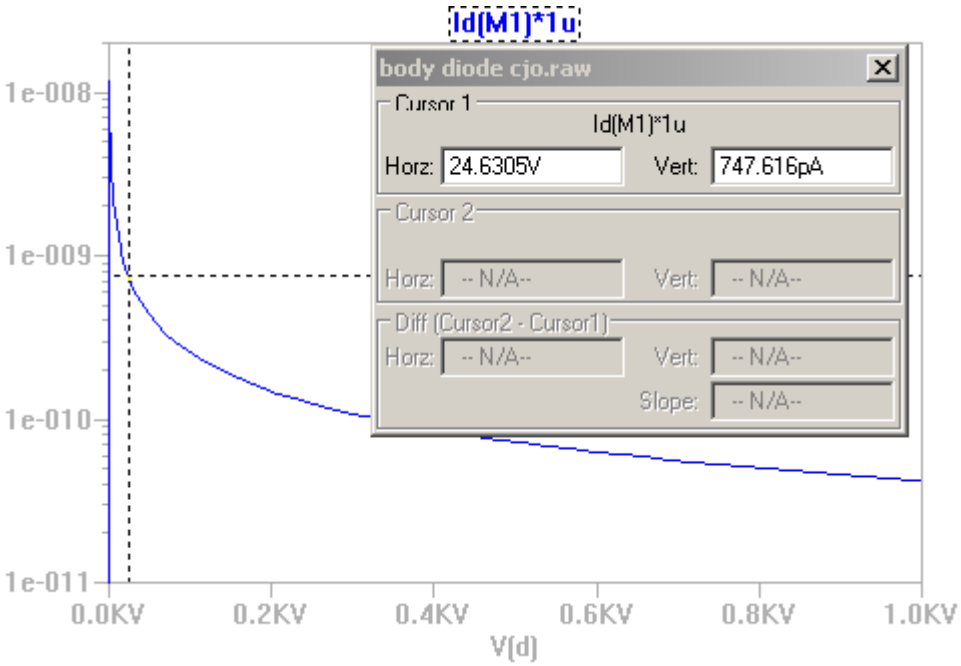
$$Cds_{25V} = Coss - \frac{Crss * (Ciss - Crss)}{Ciss}$$

## *Simulation results of the Cds*

Test setup:




Using Cjo=11.6nf and m=0.78 and Vj=0.75 the Cds as function of Vds is:
The Cgsmin and Cgsmax is set to zero to eliminate them from simulation.




The current here must be read as capacitance.

## *Summary*

The formulas generate a mosfet suitable for switching applications. The model created has some limitations regarding the DC characteristics but the Rdson and the trans-conductance is modeled correctly. Allso the gate charge and output capacitor will be an accurate match to the datasheet charges.

Here are the formulas to create a model from datasheet.

**DC parameters:**

KP = Gfs
Vto=Vgs (th)
Rs=(Vgsmax-sqrt(2*Idmax/Gfs)-Vth)/Idmax
Rd= Rdson-Rs-1/Gfs(10- Rs/Rdson -Vth)
Rg=Rg

**AC parameters**

Cgdmax=Crssmax+(Crssmax-Crssmin)/ATAN(10000)
Cdgmin=Crssmin
Cgs=Ciss-Crss
Cjo==(Cossmax-Crssmax*Cgs/(Crssmax+Cgs))

m=-LOG(Cds25V/Cjo)/LOG(1+25/0.75)

With Cds25V:

$$Cds_{25V} = Coss - \frac{Crss * (Ciss - Crss)}{Ciss}$$

To be sure set vj to 0.75 with model parameter

Vj=0.75

**Body diode DC parameters:**

$$Rb = \frac{Vd}{Id} - \frac{nkT}{Id * q} \ln\left(\frac{Id}{Is} + 1\right)$$

Is = Idss

N=1

Id and Vd are the forward voltage and current of the diode. Datasheet uses Is (Isource) for the Id and Vsd for Vd.

Regards,
Hendrik Jan Zwerver